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02/04/02

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10067441	02/04/2002	365	201	2818	11/20/02

**APPLICANTS: Kotowski Jeffrey; Fodchuk Kyle:

2824

**CONTINUING DATA VERIFIED:

NONE

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** FOREIGN APPLICATIONS VERIFIED:

NONE

PG-PUB	DO NOT PUBLISH <input checked="" type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	ATTORNEY DOCKET NO
35 USC 119 conditions met	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	NSC1-G9800 [P05051]
Verified and Acknowledged Examiners's initials <i>JH H JMH</i>		
TITLE : Integrated circuit and method for testing same using single pin to control test mode and normal mode operation		

U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
ISSUE FEE		Sheets Drwg.	Figs. Drwg.
Amount Due	Date Paid	Print Fig.	
Primary Examiner		Application Examiner	
PREPARED FOR ISSUE			
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